



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 09/997,122 | 11/28/2001 | Michael W. Johnson | 80113.0230 | 3626 |
| 20480 | 7590 | 05/07/2004 | EXAMINER | |
| STEVEN L. NICHOLS RADER, FISHMAN & GRAVER PLLC 10653 S. RIVER FRONT PARKWAY SUITE 150 SOUTH JORDAN, UT 84095 | | | LABAZE, EDWYN | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2876 | |

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/997,122

Applicant(s)

JOHNSON, MICHAEL W.

Examiner

EDWYN LABAZE

Art Unit

2876

A2

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-15 and 27-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-15 and 27-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of amendments filed on 2/25/2004.
2. Claims 1-3, 5-15, and 27-36 (including newly claims 32-36) are presented for examination. Claims 20-26 were withdrawn for consideration, and claims 4, and 16-19 cancelled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-6, 8, 10-14, 27, 29-30, and 32-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimura (U.S. 5,650,974).

Re claim 1: Yoshimura discloses semiconductor memory device and power supply control IC for use with semiconductor memory device which includes processing and memory circuitry 3 (as shown in fig. # of Yoshimura; col.8, lines 50+); an interface for electrically connecting said smart card [Yoshimura discloses that the device 1 of figs. # 8 & 9 is a memory card that is a card-like data storage; col.1, lines 15-25] to a host device 20 (col.7, lines 35+), the interface comprising a power line 100 [as seen in fig. # 1] for receiving power from the host device 20 (col.1, lines 36+); a primary battery [herein disclosed as BAT 1] disposed in the smart card 1 for providing power to the processing and memory circuitry 3 (col.8, lines 45+); and a secondary rechargeable battery [herein disclosed as BAT 1] disposed in the smart card 1 for providing power to said processing and memory circuitry 3 (col.8, lines 48+); and recharging

Art Unit: 2876

circuitry 6 for recharging the secondary battery with power from the host device (as shown in fig. # 1; col.9, lines 1+); and means for preventing [Yoshimura discloses a diode D1 for preventing the reverse current since the primary battery cannot be recharged, and through the switch SW5 for preventing the secondary battery to receive any charge/current from the primary battery. Yoshimura discloses that the switch SW5 is turned off when the primary battery BAT1 is the main battery as detected by the main battery sensor block 11 and when the voltage level supplied by the power supply VCC drops at node 100, and the host apparatus 20 is disconnected from the device (see col.10, lines 33+). Therefore the secondary battery receives no charge from the primary battery] the primary and secondary batteries from charging each other (col.8, lines 35+).

Re claims 2, 33: Yoshimura teaches an apparatus and method, wherein the primary battery is non-rechargeable (col.2, lines 3+; col.8, lines 57+).

Re claims 5, 13: Although Yoshimura does not disclose a first diode from preventing discharge of the secondary battery into the primary battery, the embodiment discloses a SW3 constructed of p-channel MOS transistors (col.4, lines 37+; col.8, lines 6+) as functionally equivalent to a diode and thereby preventing any discharge of the secondary battery into the primary battery by turning OFF upon detection of the primary. Therefore, one skilled in the art would agree that Yoshimura's teachings does disclose a means for preventing discharge of the secondary battery into the primary battery.

Re claims 6, 14: Yoshimura discloses an apparatus and method, further comprising a diode D1 preventing discharge of the primary battery BAT1 into the second battery BAT2 (col.8, lines 55+).

Re claim 8: Yoshimura teaches an apparatus and method, comprising means of providing a charged primary battery and a charged secondary battery in the smart card 1 prior to installation of the card in a host device 20 (in order words using/installing two new batteries in the card); determining [through the MBOUT 11 and the battery voltage comparator 23] whether the primary or secondary battery has a higher voltage prior to installation of the card in host device 20 (col.13, lines 1+); and providing power to processing memory and circuitry 3 with whichever battery has the higher voltage prior to installation of the card in the host device (col.13, lines 25+).

Re claim 10: Yoshimura discloses an apparatus and method, further comprising installing the smart card 1 in a host device 20 (col.7, lines 35+); electrically connecting [through contacts 28] the smart card to the host device 20 (col.14, lines 21+) and providing power to the smart card 1 from the host device 20 (col.); and charging [through charging circuit 6] the secondary battery with power from the host device 20 (col.15, lines 50-67).

Re claim 11: Yoshimura teaches an apparatus and method, further comprising providing power to the processing and memory circuitry 8 with the second battery BAT2 when the card is removed from the host device 20 (col.8, lines 48+; col.9, lines 38-58; col.11, lines 38+).

Re claims 12, 29: Yoshimura discloses an apparatus and method, further comprising charging [through the charging circuit 6] the secondary battery prior to installation of said smart card in a host device 20 (col.15, lines 50-67); and powering the processing and memory circuitry 3 with the secondary battery after depletion of the primary battery [by using the battery voltage comparator 23 to compare with the voltage level of the first battery BAT1 and if the voltage

Art Unit: 2876

level drops, then switch to voltage node 103 to connect the second battery BAT2 so as to supply power to the processing and memory circuitry 3] (col.13, lines 1-32).

Re claim 27: Yoshimura teaches an apparatus and method, comprising of means of providing power to the processing and memory circuitry 3 with a primary non-rechargeable battery BAT1 [as the main battery] disposed in the smart card 10 prior to installation of the smart card 10 in a host device 20 (col.11, lines 1+), charging [through charging circuit 6] a secondary rechargeable battery BAT2 with power from the host device 20 when the smart card 10 is installed in the host device 20 (col.15, lines 50-67); and providing power to the processing and memory circuitry with the secondary battery when the primary battery is depleted and the smart card is removed from the host device [by using the battery voltage comparator 23 to compare with the voltage level of the first battery BAT1 and if the voltage level drops, then switch to voltage node 103 to connect the second battery BAT2 so as to supply power to the processing and memory circuitry 3] (col.13, lines 1-32).

Re claim 30: Yoshimura discloses an apparatus and method, further comprising means of preventing discharge of the secondary battery BAT2 [through the switch SW5] into the primary battery BAT1 (col.10, lines 33+; col.11, lines 27+); and preventing discharge of the primary battery BAT1 [through the diode D1] into the secondary battery BAT2 (col.8, lines 55+).

Re claim 32: Yoshimura teaches an apparatus, further comprising charging the secondary rechargeable battery BAT2 with power from the host device 10 when the smart card is installed in the host device 20 (col.9, lines 18-37; col.10, lines 40+).

Re claim 34: Yoshimura discloses an apparatus and method, further comprising periodically determining [through the battery voltage comparator 5/23] whether the primary or

Art Unit: 2876

secondary battery has a higher voltage prior to installation of the smart card 10 in the host device 20 (col.8, lines 23+); and providing power to the processing and memory circuitry 8 with whichever battery has the higher voltage prior to installation of the smart card 10 in the host device 20 (col.9, lines 22+; col.12, lines 20-67).

Re claim 35: Yoshimura teaches an apparatus and method, further comprising switching which of the two the batteries provides power to the processing and memory circuitry 3 when a voltage of the battery supplying power drops below a voltage of the battery not supplying power (col.10, lines 25-67; col.13, lines 15+).

Re claim 36; Yoshimura discloses an apparatus and method, further comprising, if the primary and secondary batteries have an equal voltage, supplying power to the processing and memory circuitry 8 with both the primary and secondary batteries (col.2, lines 47+).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3, 9, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (U.S. 5,650,974) in view of Reyes (U.S. 5,818,030).

The teachings of Yoshimura have been discussed above.

Yoshimura fails to teach that the primary battery is a lithium battery.

Art Unit: 2876

Reyes discloses credit card system with key module with includes a lithium battery P (col.8, lines 7-43).

In view of Reyes' teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ into the teachings of Yoshimura a lithium battery as the primary battery for durability and large power capacities (as disclosed by Yoshimura in col.8, lines 45+). Furthermore, the lithium battery consumes minimal power during transmission and reception, can be made of very thin film [represents a space-saver], and has long-lasting operating life. Moreover, such modification would have been an obvious extension as taught by Yoshimura, therefore an obvious expedient.

7. Claims 7, 15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (U.S. 5,650,974) in view of Ben-David (US 2002/0154137).

The teachings of Yoshimura have been discussed above.

Yoshimura fails to teach access control data for a cable television system stored in the processing and memory circuitry.

Ben-David teaches transmission of digital data from a screen, which includes a smart card 84 to access control data for a cable television system 24 (as shown in figs. # 10 & 12 of Ben-David; col.6, paragraphs 0077 to paragraph 0095).

In view of Ben-David's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ into the teachings of Yoshimura a means of accessing control data for the cable television system from the semiconductor memory device of Yoshimura. Furthermore, since the card of Yoshimura is required to store data onto the memory 3 and wherein the host device 20 could be a cable television system [as of the teachings

Art Unit: 2876

of Ben-David], therefore such semiconductor device/smart card could be used to access control data for a cable television system. Moreover, such modification would have been an obvious extension as taught by Yoshimura.

Response to Arguments

8. Applicant's arguments with respect to claims 1-3, 5-15, and 27-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Larson et al. (U.S. 6,109,530) discloses integrated circuit carrier package with battery coin cell.

Schnell et al. (U.S. 6,239,578) teaches system and method for preservation of battery power during reconditioning.

Atsmon et al. (US 2004/0031856) discloses physical presence digital authentication system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (571) 272-2395.

The examiner can normally be reached on 7:30 AM - 4:00 PM.

Art Unit: 2876

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

el
Edwyn Labaze
Patent Examiner
Art Unit 2876
April 30, 2004



THIEN M. LE
PRIMARY EXAMINER